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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,433	02/28/2002	Yves L. Baeyens	Baeyens 1-24-4-1-1	3191
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MENDELSON & ASSOCIATES, P.C. 1500 JOHN F. KENNEDY BLVD., SUITE 405 PHILADELPHIA, PA 19102			EXAMINER SEDIGHIAN, REZA	
			ART UNIT	PAPER NUMBER
			2613	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/085,433

Applicant(s)

BAEYENS ET AL.

Examiner

M. R. Sedighian

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-17 and 19-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24 and 25 is/are allowed.
- 6) ☒ Claim(s) 1,3-5,8-9,13,14,17,19,22,23 and 26-31 is/are rejected.
- 7) ☒ Claim(s) 6,7,10-12,15,16,20 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. This communication is responsive to applicant's 3/16/06 remarks and arguments.

Claims 1, 3-17, and 19-31 are now pending.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3-5, 9, 13-14, 17, 19, 22-23, and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Givehchi (US Patent Application Publication No: 2002/0109893 A1) in view of Nagata (US Patent No: 6,114,981).

Regarding claims 1 and 17, Givehchi teaches an apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal (page 1, paragraph 0013, page 2, paragraph 0018), comprising: an amplifier configured to generate an amplified RZ data signal corresponding to the NRZ data signal (page 1, paragraph 0007) based on (i) the NRZ data signal and (ii) a clock signal synchronized with the NRZ data signal (page 1, paragraph 0007, lines 12-15), wherein the amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal (page 2, paragraph 0016, lines 7-17). Givehchi differs from the claimed invention in that Givehchi does not specifically disclose there is a DC offset between the first and second signals. Nagata teaches a signal generator (2, fig. 1) that receives a NRZ signal (NRZ, fig. 1) and a clock signal (CK, fig. 1) to further generate a RZ signal (RZ, fig. 1), wherein a modulator (1, fig. 1) receives a multi-bit signal to which a DC

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offset value is added to output the NRZ signal (see abstract). As it is taught by Nagata, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a DC offset input signal as the first signal or as the input data signal, or to provide a DC offset signal to the input data signal such as the one of Nagata, for the input data, in the data generator circuit of Givehchi to provide a data signal having an offset phase with respect to phase of the clock signal.

Regarding claims 3 and 19, Givehchi teaches the first signal is an NRZ data signal (page 3, paragraph 0018).

Regarding claim 4, Givehchi teaches the width of pulses representing data in the amplified RZ data signal is controlled by a DC value (page 3, paragraph 0019).

Regarding claim 5, Givehchi teaches the circuitry configured to condition at least one of the NRZ data signal and the clock signal to produce at least one of the first and second signals (page 3, paragraph 0020 and fig. 3).

Regarding claim 9, Givehchi teaches the apparatus is implemented as an integrated circuit (page 3, paragraph 0020).

Regarding claim 13, Givehchi teaches the apparatus further comprises an electro-optic modulator (202, fig. 2) configured to receive an optical input (201, fig. 2) from a laser (230, fig. 2) and to modulate the optical input using the amplified RZ data signal to output an optical RZ data signal corresponding to the amplified RZ data signal (page 2, paragraph 0016).

Regarding claim 14, Givehchi teaches a laser that generates a continuous light emission (CW 230, fig. 2).

Regarding claims 22-23, Givehchi teaches a circuit (240, fig. 2) adapted to generate a sinusoidal signal, the sinusoidal signal being the clock signal synchronized with the NRZ data signal (page 3, paragraph 0020 and fig. 3).

Regarding claims 26 and 29, as to a fixed DC offset between the first and second signals, Nagata teaches a DC offset can be added to the input data (fig. 7). It would have been obvious that such DC offset can be a fixed DC offset to provide the desired signal shift.

Regarding claims 27 and 30, Givehchi teaches the second signal has a substantially constant amplitude (page 2, paragraph 0018 and fig. 3, note that the amplitude of the clock signal can be constant).

Regarding claims 28 and 31, Givehchi teaches the second signal does not carry data (the second signal is the clock signal).

4. Claims 1, 3-5, 8-9, 13-14, 17, 19, 22-23, and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walklin (US Patent Application Publication No: 2002/0171903 A1) in view of Nagata (US Patent No: 6,114,981).

Regarding claims 1 and 17, Walklin teaches an apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal (page 1, paragraph 0001), comprising: an amplifier (32, fig. 3A) configured to generate an amplified RZ data signal corresponding to the NRZ data signal (page 2, paragraph 0032) based on (i) the NRZ data signal (S_{NRZ} , fig. 3A) and (ii) a clock signal synchronized (CK, fig. 3A) with the NRZ data signal, wherein the amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a

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second signal corresponding to the clock signal (page 2, paragraph 0032). Walklin differs from the claimed invention in that Walklin does not specifically disclose there is a DC offset between the first and second signals. Nagata teaches a signal generator (2, fig. 1) that receives a NRZ signal (NRZ, fig. 1) and a clock signal (CK, fig. 1) to further generate a RZ signal (RZ, fig. 1), wherein a modulator (1, fig. 1) receives a multi-bit signal to which a DC offset value is added to output the NRZ signal (see abstract). As it is taught by Nagata, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a DC offset input signal as the first signal or as the input data signal, or to provide a DC offset signal to the input data signal such as the one of Nagata, for the input data, in the data converter of Walklin to provide a data signal having an offset phase with respect to phase of the clock signal.

Regarding claims 3 and 19, Walklin teaches the first signal is an NRZ data signal (S_{NRZ} , fig. 3A).

Regarding claim 4, Nagata teaches the width of pulses representing data is controlled by a DC value (col. 2, lines 39-47 and figs. 6, 7).

Regarding claim 5, Walklin teaches the circuitry configured to condition at least one of the NRZ data signal and the clock signal to produce at least one of the first and second signals (page 2, paragraph 0032).

Regarding claim 8, Walklin teaches an amplification stage (32). Walklin differs from the claimed invention in that Walklin does not specifically disclose two or more amplification stages. However, it would have been obvious to a person of ordinary skill in the art to provide more amplification stages, such as the amplification stage 32, in the data transmission system of Walklin to further amplify and boost the signal strength.

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Regarding claim 9, Walklin teaches the apparatus is implemented as an integrated circuit (31, 2, fig. 3A).

Regarding claim 13, Walklin teaches the apparatus further comprises an electro-optic modulator (2, fig. 3A) configured to receive an optical input from a laser (1, fig. 3A) and to modulate the optical input using the amplified RZ data signal (S_{drive} , fig. 3A) to output an optical RZ data signal (O_{RZ} , fig. 3A) corresponding to the amplified RZ data signal.

Regarding claim 14, Walklin teaches a laser that generates a continuous light emission (CW laser, fig. 3A).

Regarding claims 22-23, Walklin teaches a circuit adapted to generate a sinusoidal signal, the sinusoidal signal being the clock signal (CK, fig. 3A) synchronized with the NRZ data signal (S_{NRZ} , fig. 3A).

Regarding claims 26 and 29, as to a fixed DC offset between the first and second signals, Nagata teaches a DC offset can be added to the input data (fig. 7), as it is discussed above. It would have been obvious that such DC offset can be a fixed DC offset to provide the desired signal shift.

Regarding claims 27 and 30, Walklin teaches the second signal has a substantially constant amplitude (note that the amplitude of the clock signal can be constant).

Regarding claims 28 and 31, Walklin teaches the second signal does not carry data (the second signal is the clock signal).

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5. Claims 6-7, 10-12, 15-16, and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 24-25 are allowed.

7. Applicant's arguments filed 3/16/06 have been fully considered but they are not persuasive.

Remark states in the Nagata's fig. 7, the DC offset is added to the multi-bit input signal applied to $\Sigma\Delta$ modulator 1, and not to the NRZ output signal applied to AND circuit 12. Claim 1 of present application recites "... a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal; and there is a DC offset between the first and second signals". Nagata teaches a signal generator 2 that receives a NRZ data signal and a CK signal, wherein the NRZ signal corresponds to a multi-bit digital signal (or a first signal) that is shifted by a DC offset value (col. 8, lines 4-5 and fig. 7). Accordingly, a first signal (or the multi-bit digital signal) that corresponds to NRZ data signal has a DC offset value, as recited in claim 1. Note that claims 1 and 17, each requires a DC offset between a first and second signal, wherein the first signal corresponds to the NRZ data signal. Nagata clearly teaches a first signal with an added DC offset (the multi-bit digital signal inputted to the $\Sigma\Delta$ modulator 1) that corresponds to a NRZ data signal and a second signal (the CK signal). Applicant's attention is directed that during the prosecution of a pending patent application, the terms found in the claims should be given the broadest reasonable interpretation, See *In re Pearson*, 181 USPQ 641 (CCPA 1974).

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8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. R. Sedighian whose telephone number is (571) 272-3034. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


M. R. SEDIGHIAN
PRIMARY EXAMINER